



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Diorio et al.
SERIAL NO.: 10/681,577
FILING DATE: October 7, 2003
TITLE: USE OF ANALOG-VALUED FLOATING-GATE TRANSISTORS
TO MATCH THE ELECTRICAL CHARACTERISTICS OF
INTERLEAVED AND PIPELINED CIRCUITS
EXAMINER: [not yet assigned]
ART UNIT: [not yet assigned]

CERTIFICATE OF MAILING

I hereby certify that this paper is being deposited with the United States Postal Service as First Class
Mail in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the date
printed below:

Date: 1-9-04

Name: Diane Morse
Diane Morse

COMMISSIONER FOR PATENTS
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ALEXANDRIA, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Each item of information listed in the attached FORM PTO-1449, for which a
copy of each is attached, may be material to the examination of the above-identified
application and is, therefore, submitted in compliance with the duty of disclosure defined
in 37 CFR §§ 1.56, 1.97 and 1.98. The Examiner is requested to make these items of
official record in this application.

This Information Disclosure Statement under 37 CFR §§ 1.56, 1.97 and 1.98 is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that any one or more of these items constitutes prior art.

I

This statement is filed pursuant to:

(X) 37 C.F.R. § 1.97(b).

This information disclosure statement is filed either (1) within three months of the filing date of a national application other than a continued prosecution application under §1.53(d); (2) within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application; (3) before the mailing date of a first office action on the merits, or (4) before the mailing of a first office action after the filing of a Request for Continued Examination under 37 C.F.R. § 1.114, whichever event occurs last.

Accordingly, this information disclosure statement requires no fee and no certification.

() 37 C.F.R. § 1.97(c).

This information disclosure statement is filed after the period specified in 37 C.F.R. § 1.97 (b), but before the mailing date of either (1) a final action under 37 C.F.R. § 1.113; (2) a notice of allowance under 37 C.F.R. § 1.311; or (3) an action that otherwise closes prosecution in the application.

Accordingly, this information disclosure statement requires either the fee specified in 37 C.F.R. § 1.17 (p) for submission of an information disclosure statement under 37 C.F.R. § 1.97 (c) (\$180); or a certification according to 37 C.F.R. § 1.97 (e).

() 37 C.F.R. § 1.97(d).

This information disclosure statement is filed after the period specified in 37 C.F.R. § 1.97 (c).

Accordingly, this information disclosure statement requires the fee specified in 37 C.F.R. § 1.17 (p) to consider an information disclosure statement under 37 C.F.R. § 1.97(d) (\$180), and a certification according to 37 C.F.R. § 1.97(e).

If this statement crosses in the mail with an office action, or is otherwise not in the indicated category of 37 C.F.R. § 1.97, it is respectfully requested that this statement be treated in the next appropriate category and made of record. To the extent required, please treat this paper as a conditional petition for acceptance of the information disclosure statement.

II

- (X) No fee is due.
- () The fee specified in 37 C.F.R. § 1.17(p) for submission of an information disclosure statement under 37 C.F.R. § 1.97(c) is enclosed (\$180).

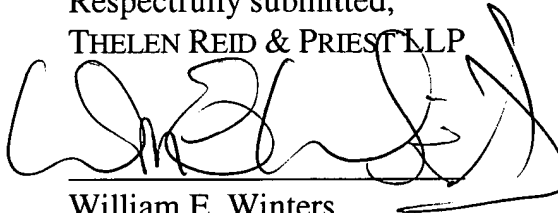
Please charge any additional required fee or credit any overpayment to our deposit account number 50-1698. An additional copy of this page is enclosed.

III

Pursuant to 37 C.F.R. § 1.97(e), I certify:

- (X) No certification is necessary.
- () (1) Each item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the statement.
- () (2) No item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, or, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c), more than three months prior to the filing of the statement.

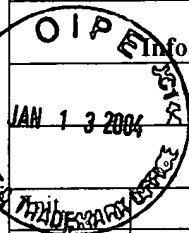
Respectfully submitted,
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Dated: January 9, 2004

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Form PTO 1449 (Rev. 2-32) U.S. Department of Commerce Patent and Trademark Office				Atty. Docket No. IMPJ-0004		Serial No. 10/681,577		
 Information Disclosure Statement by Applicant (Use several sheets if necessary)				Applicant: Diorio et al.				
				Filed: 10/7/03 Group: Unknown				
U.S. Patent Documents								
		Document No.	Date	Name	Class	Subclass	Filing Date	
	A	4,763,105	08/09/88	Jeng	340	347	07/08/87	
	B	4,962,380	10/09/90	Meadows	341	120	09/21/89	
	C	4,968,988	11/06/0	Miki et al.	341	141	11/22/88	
	D	5,270,963	12/14/93	Allen et al.	364	861	07/06/90	
	E	5,627,392	05/06/97	Diorio et al.	257	315	03/07/95	
	F	5,825,063	10/20/98	Diorio et al.	257	316	07/26/96	
	G	5,875,126	02/23/99	Minch et al.	365	185.01	09/26/96	
	H	5,898,613	04/27/99	Diorio et al.	365	185.03	06/25/97	
	I	5,914,84	06/22/99	Diorio et al.	365	185.03	06/01/98	
	J	5,986,927	11/16/99	Minch et al.	365	185.01	11/10/98	
	K	5,990,512	11/23/99	Diorio et al.	257	314	04/22/97	
	L	6,125,053	09/26/00	Diorio et al.	365	185.03	11/30/98	
	M	6,144,581	11/07/00	Diorio et al.	365	185.03	11/30/98	
	N	6,664,909	12/16/03	Hyde et al.	341	144	08/13/01	
Foreign Documents								
							Translation	
Init.		Document No.	Date	Country	Class	Subclass	Yes	No
Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)								
	O	Diorio et al., "Adaptive CMOS: From Biological Inspiration to Systems-on-a-Chip", March 2002, Proceedings of the IEEE, Vol. 90, No. 3, p. 345-357.						
	P	Figueroa et al., "A Floating-Gate Trimmable High-Resolution DAC in Standard 0.25µm CMOS", August 2001, Nonvolatile Semiconductor Memory Workshop, Monterey, CA, pp. 46-47.						
	Q	Hyde et al., "A Floating-Gate Trimmed, 14-Bit, 250 Ms/s Digital-to-Analog Converter in Standard 0.25µm CMOS", 2002, Symposium on VLSI Circuits, Honolulu, HI, pp. 328-331.						
Examiner					Date Considered			
Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with the next communication to applicant.								